Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **1Y**
2. **1A**
3. **1B**
4. **2Y**
5. **2A**
6. **2B**
7. **GND**
8. **3A**
9. **3B**
10. **3Y**
11. **4A**
12. **4B**
13. **4Y**
14. **VCC**

**52 mils**

**50 mils**

**54AS00**

**A**

**MASK**

**REF**

**2 1 14 13**

**12**

**11**

**10**

**6 7 8 9**

**3**

**4**

**5**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .005” X .005”**

**Backside Potential:**

**Mask Ref: 54AS00 A**

**APPROVED BY: DK DIE SIZE .052” X .057” DATE: 6/6/16**

**MFG: TEXAS INSTRUMENTS THICKNESS .011” P/N: 54AS02**

**DG 10.1.2**

#### Rev B, 7/19/02